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(54) SOLID-STATE IMAGE PICKUP ELEMENT

(57)Abstract:
PURPOSE: To suppress blooming at the time of high luminance object image pickup and to obtain improved images over the wide range of illuminance by discharging excessive charge generated in a photoelectric conversion element part from the source side of a MOS transistor for reset.
CONSTITUTION: In a storage mode in which a photoelectric conversion element 1 integrates signal charge generated by incident light, by the driver circuit 12b of a vertical scanning circuit 12, a power supply line 12c is turned to a high level VR (H), a 12d is turned to a low level potential VR (L) and a voltage equal to or more than a threshold value is applied through a vertical selection line 9 for reset to the gate of the MOS transistor 4 for reset serially connected to the photoelectric conversion element 1. Thus, the MOS transistor 4 for reset is turned to an ON state during a storage period, the excessive charge generated in the photoelectric conversion element 1 is discharged to the source side and the blooming is suppressed.

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CLAIMS

[Claim(s)]

[Claim 1] The 1st MOS transistor for reset which made the source field the optoelectric-transducer section, The 2nd MOS transistor for magnification read-out by which the gate was connected to the above-mentioned optoelectric-transducer section, In the solid state image sensor equipped with two or more pixels which have the 3rd MOS transistor for pixel selection connected to the 2nd MOS transistor of the above at the serial The solid state image sensor characterized by equipping the gate of the 1st MOS transistor of the above with a scan means to impress the electrical potential difference more than the threshold of this MOS transistor, at the time of the charge storage of the above-mentioned optoelectric-transducer section.

[Claim 2] The solid state image sensor according to claim 1 characterized by constituting the 1st MOS transistor of the above from a depression transistor.

[Claim 3] The solid state image sensor according to claim 1 with which

channel concentration of the 1st MOS transistor of the above is characterized by being equal to the concentration of a substrate or a well.

[Claim 4] The solid state image sensor according to claim 1 characterized by the gate length of the 1st MOS transistor of the above consisting of minimum line width.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] Especially this invention relates to the improvement of a magnification read-out mold solid state image sensor about a solid state image sensor.

[0002]

[Description of the Prior Art] Conventionally, in connection with horizontal high-resolution-izing and densification, the area per pixel in image sensors reduces image sensors, and the quantity of light which carries out incidence to per pixel is decreasing. Therefore, the reinforcement of the signal read from image sensors fell, and the fall of a S/N ratio (S is a signal and N is a noise) is caused. In order to conquer such a problem, it is thought desirable to use the image sensors of a magnification read-out mold.

[0003] Drawing 9 is the circuit diagram showing a typical example of the conventional magnification read-out mold image sensors. While these image sensors are equipped with two or more the optoelectric transducer 1 formed by the PN junction, MOS transistors 2 for magnification read-out, MOS transistors 3 for pixel selection by which the gate was connected to the perpendicular selection line, and MOS transistors 4 for reset of an optoelectric transducer 1 as 1 pixel Those functional devices 1-4 To the included pixel, a power source The level power-source line 5 to supply and the pixel arranged perpendicularly The I/V conversion amplifier 10 for changing into an electrical potential difference MOS transistor 8 for level selection for choosing the perpendicular selection line 6 for choosing, the perpendicular signal line 7 arranged perpendicularly, and the pixel arranged horizontally, the level signal line 13, and the signal current, the horizontal scanning circuit 11, And it has the vertical-scanning circuit 12.

[0004] Drawing 10 is a circuit diagram for explaining actuation of one pixel of the arbitration of the image sensors shown in drawing 9 . In addition, although the perpendicular selection line 9 for reset was shared with the perpendicular selection line 6 of the following line with the configuration of drawing 9 mentioned above in order to reduce the number of wiring arranged in a pixel array and to raise a degree of integration The signal in each location which separated and showed the perpendicular selection line 9 for reset and the perpendicular selection line 6 of the following line, and was expressed with various reference marks is expressed with the configuration of drawing 10 using the same reference mark as drawing 9 .

[0005] Moreover, drawing 11 is a timing chart for explaining actuation of the 1-pixel circuit shown in drawing 10 . In drawing 11 , period 1H are 1 level period in the usual television method, and a horizontal blanking interval and period Read-out are equivalent to a signal read-out period for period H-BLK. Moreover, the clock V1 and the clock H1 express typically the clock supplied to the vertical-scanning circuit 12 and the horizontal scanning circuit 11, respectively.

[0006] In the time of day T0 shown in drawing 11 , potential of the level power-source line 5 shown by the perpendicular selection line 6 shown by VS and VL is now made high-level, and MOS transistor 2 for magnification read-out and MOS transistor 3 for perpendicular selection have become switch-on. Since the outgoing end of an optoelectric transducer 1 is connected to the gate electrode of above-mentioned MOS transistor 2 for magnification read-out, MOS transistor 2 for magnification read-out is switch-on with the impedance depending on the output potential Vpd of an optoelectric transducer 1. Then, the signal current Isig corresponding to [if the i-th output signal Hi from the horizontal scanning circuit 11 will become high-level and MOS transistor 8 for level selection will be in switch-on in the time of day T1 in read-out period Read-out, the perpendicular signal line 7 will be electrically connected to the I/V conversion amplifier 10, and] the output potential Vpd of an optoelectric transducer 1 It will be read as a voltage signal.

[0007] It is voltage-level Vreset to which an optoelectric transducer 1 is supplied from the level power-source line 5 through MOS transistor 3 for perpendicular selection, and MOS transistor 4 for reset by the potential of the perpendicular selection line 9 for reset shown by VR becoming high-level in the time of day T2 within the next horizontal blanking interval. It is reset. And an optoelectric transducer 1 goes into the are recording mode in which it integrates with the signal

charge generated depending on incident light, from time-of-day T3 within the next horizontal blanking interval.
[0008]
[Problem(s) to be Solved by the Invention] Since the conventional magnification mold image sensors are constituted as mentioned above, the area per pixel in image sensors is reduced and high integration is attained, at the time of a high brightness photographic subject image pick-up The signal charge generated in a pixel by excessive incident light became superfluous, and there was a trouble that the superfluous charge was contained into a contiguity pixel, and light was contained also in a part for overflow and the picture element part by which light originally is not irradiated and of spoiling image quality according to that so-called blooming phenomenon [like].
[0009] This invention was made in order to cancel the above troubles, it controls the blooming at the time of a high brightness photographic subject image pick-up, and aims at obtaining the solid state image sensor with which a good image is obtained in a wide range illuminance.
[0010]
[Means for Solving the Problem] The 1st MOS transistor for reset to which the solid state image sensor concerning claim 1 of this invention made the source field the optoelectric-transducer section, The 2nd MOS transistor for magnification read-out by which the gate was connected to the above-mentioned optoelectric-transducer section, In the solid state image sensor equipped with two or more pixels which have the 3rd MOS transistor for pixel selection connected to the 2nd MOS transistor of the above at the serial It is characterized by equipping the gate of the 1st MOS transistor of the above with a scan means to impress the electrical potential difference more than the threshold of this MOS transistor, at the time of the charge storage of the above-mentioned optoelectric-transducer section.
[0011] Moreover, the solid state image sensor concerning claim 2 is characterized by constituting the 1st MOS transistor of the above from a depression transistor.
[0012] Moreover, the solid state image sensor concerning claim 3 is characterized by the channel concentration of the 1st MOS transistor of the above being equal to the concentration of a substrate or a well.
[0013] Furthermore, the solid state image sensor concerning claim 4 is characterized by the gate length of the 1st MOS transistor of the above consisting of minimum line width.
[0014]
[Function] In the solid state image sensor concerning claim 1 of this

invention With a scan means, by impressing the electrical potential difference more than the threshold of this MOS transistor to the gate of the 1st MOS transistor for reset at the time of the charge storage of the optoelectric-transducer section A blooming is controlled, as during an are recording period changes the 1st MOS transistor for resetting the optoelectric-transducer section into ON condition and the superfluous charge generated in the optoelectric-transducer section is drawn out from the source side of the 1st MOS transistor for reset.

[0015] Moreover, in the solid state image sensor concerning claim 2, by constituting the 1st MOS transistor of the above from a depression transistor, the electrical potential difference impressed to the gate can be made into a grand level, and it becomes possible to make the power-source line unnecessary.

[0016] Moreover, in the solid state image sensor concerning claim 3, by making channel concentration of the 1st MOS transistor of the above equal to the concentration of a substrate or a well, a threshold electrical potential difference can be decided by the concentration, and reset dispersion is reduced.

[0017] Furthermore, in the solid state image sensor concerning claim 4, contraction of a pixel dimension is enabled by constituting the gate length of the 1st MOS transistor of the above from minimum line width.

[0018]

[Example]

The example 1 of this invention is explained about drawing below example 1. First, although it has the same configuration as the 1-pixel circuit shown in the configuration and drawing 10 of the image sensors shown in drawing 9 concerning the conventional example in this example 1 In the circuit diagram shown in drawing 10 , the circuitry of the output section of the perpendicular selection line 9 for reset in the vertical-scanning circuit 12 differs. By impressing the electrical potential difference more than the threshold of this MOS transistor 4 to the gate of MOS transistor 4 for reset at the time of the charge storage of an optoelectric transducer 1 A blooming is controlled, as during an are recording period changes MOS transistor 4 for reset of an optoelectric transducer 1 into ON condition and the superfluous charge generated in the optoelectric transducer 1 is drawn out from the source side of MOS transistor 4 for reset.

[0019] That is, drawing 1 is the circuitry Fig. showing the output section of the perpendicular selection line 9 for reset in the vertical-scanning circuit 12 in a detail in the 1-pixel circuitry Fig. which starts an example 1 and is shown in drawing 10 . In drawing 1 , the MOS

transistor for pixel selection to which 1 thru/or 12 showed the same part as drawing 10 , as for the optoelectric transducer in which 1 was formed by the PN junction, and 2, the MOS transistor for magnification read-out was connected to the perpendicular selection line, and, as for 3, the gate was connected, and 4 are the MOS transistors for reset of an optoelectric transducer 1, and constitute 1 pixel of image sensors by these. Moreover, the level power-source line which supplies a power source to the pixel in which 5 contains those functional devices 1-4, A perpendicular selection line for 6 to choose the pixel arranged perpendicularly, the perpendicular signal line with which 7 has been arranged perpendicularly, The MOS transistor for level selection for 8 to choose the pixel arranged horizontally, As for a horizontal scanning circuit and 12, I/V conversion amplifier for 10 to change the signal current into an electrical potential difference and 11 are [a vertical-scanning circuit and 13] level signal lines. As circuitry of the output section of the perpendicular selection line 9 for reset in the above-mentioned vertical-scanning circuit 12 The shift register with which 12a sends out a shift pulse, the driver circuit where 12b becomes with the inverter of the p channel MOS transistor Qp and the n channel MOS transistor Qn, It is the 2nd power-source line for supplying the 1st power-source line for 12c supplying the high-level potential VR (H) to the perpendicular selection line 9 for reset, and 12d (L) of potentials VR of a low level to the above-mentioned perpendicular selection line 9 for reset. The potential of this 2nd power-source line VR (L) is set up more than the threshold of MOS transistor 4 for reset.

[0020] Moreover, drawing 2 is a timing chart for explaining actuation of an example 1, and drawing 3 shows the cross section and potential flow chart of MOS transistor 4 for reset for explaining actuation of an example 1, and explains hereafter actuation of the image sensors which start an example 1 with reference to drawing 2 and drawing 3 . In addition, in drawing 2 , period 1H are 1 level period in the usual television method, and a horizontal blanking interval and period Read-out are equivalent to a signal read-out period for period H-BLK. Moreover, the clock V1 and the clock H1 express typically the clock supplied to the vertical-scanning circuit 12 and the horizontal scanning circuit 11, respectively. Moreover, in drawing 3 , (A) is the cross section of MOS transistor 4 for reset, gate 4a of MOS transistor 4 for reset is connected to the perpendicular selection line 9 for reset, drain 4b is connected to the level power-source line 5, respectively, and the source field has become an optoelectric transducer 1. Moreover, 4c shows the substrate.

[0021] It is voltage-level Vreset to which it operates in drawing 2 now like [time of day T0 to T2] the conventional example, and an optoelectric transducer 1 is supplied from the level power-source line 5. It is reset (refer to drawing 3 (D)). That is, in the time of day T0 shown in drawing 2 , potential of the level power-source line 5 shown by the perpendicular selection line 6 shown by VS and VL is made high-level, and MOS transistor 2 for magnification read-out and MOS transistor 3 for perpendicular selection have become switch-on. Since the outgoing end of an optoelectric transducer 1 is connected to the gate electrode of above-mentioned MOS transistor 2 for magnification read-out, MOS transistor 2 for magnification read-out is switch-on with the impedance depending on the output potential Vpd of an optoelectric transducer 1.
[0022] Then, the signal current Isig corresponding to [if the i-th output signal Hi from the horizontal scanning circuit 11 will become high-level and MOS transistor 8 for level selection will be in switch-on in the time of day T1 in read-out period Read-out, the perpendicular signal line 7 will be electrically connected to the I/V conversion amplifier 10, and] the output potential Vpd of an optoelectric transducer 1 It will be read as a voltage signal. It is voltage-level Vreset to which an optoelectric transducer 1 is supplied from the level power-source line 5 through MOS transistor 3 for perpendicular selection, and MOS transistor 4 for reset by the potential of the perpendicular selection line 9 for reset shown by VR becoming high-level in the time of day T2 within the next horizontal blanking interval. It is reset.
[0023] And an optoelectric transducer 1 goes into the are recording mode in which it integrates with the signal charge generated depending on incident light, from time-of-day T3 (refer to drawing 3 (B)). When setting a SURESHI hold (threshold) electrical potential difference when the backgate of MOS transistor 4 for reset is not impressed at this time to Vthr (0), the potential potential of gate 4a of MOS transistor 4 for reset is set as the potential of the low level VR of the perpendicular selection line 9 for reset (L) so that it may be set to VR(L) >Vthr (0). As shown in drawing 1 , namely, the potential of the perpendicular selection line 9 for reset By driver circuit 12b which becomes with an inverter, to the timing reversed to the n+1st shift pulses of shift register 12a It becomes the high-level potential VR of 1st power-source line 12c (H), and the potential VR of the low level of 12d of 2nd power-source line (L). At the time of are recording mode The electrical potential difference more than the potential VR of the low level set up by 12d of 2nd power-source line (L), i.e., the threshold electrical potential difference of MOS transistor 4 for reset, is impressed to the

gate of MOS transistor 4 for reset.
[0024] therefore, the potential potential of an optoelectric transducer 1, i.e., source potential phiPD of MOS transistor 4 for reset phiPD>VR(L)-Vthr (phiPD) (Vthr (phiPD)) At the time of the SURESHI hold electrical potential difference at the time of backgate impression If the usual are recording actuation is performed and MOS transistor 4 for reset serves as phiPD<VR(L)-Vthr (phiPD) in order to cut off MOS transistor 4 for reset should turn on, and a superfluous charge should lengthen it to drain 4b, and it should blunder to it. When MOS transistor 4 for reset works as an overflow drain, (drawing 3 (c) and referring to [of drawing 2] the time-of-day T four), and a superfluous charge do not spread to a contiguity pixel, and a blooming is controlled.
[0025] Here, the amount Qmax of the maximum stored charge of an optoelectric transducer 1 is {Vreset. - (decided by VR(L)-Vthr(L)}/CPD.) CPD; Vthr which fills capacity Vthr(L);phiPD=VR(L)-Vthr (phiPD) of an optoelectric transducer 1 (phiPD)
[0026] According to the above-mentioned example 1, to therefore, the gate of MOS transistor 4 for reset which carried out the series connection to the optoelectric transducer 1 at the time of are recording mode Since it was made to impress the electrical potential difference more than the threshold electrical potential difference of MOS transistor 4 for reset set up by 12d of 2nd power-source line During an are recording period changes MOS transistor 4 for reset into ON condition, as the superfluous charge generated in the optoelectric transducer 1 is drawn out to the source side of MOS transistor 4 for reset, a blooming is controlled, and a good image is obtained in a wide range illuminance.
[0027] Example 2., next an example 2 are explained. The part as the example 1 which shows the 1-pixel circuit diagram concerning an example 2, and is shown in drawing 10 with the same drawing 4 attaches the same sign, and the explanation is omitted. In the 1-pixel circuit diagram concerning this example 2 As shown in drawing 4 , the gate of MOS transistor 4 for reset is connected to the level power-source line 5 shown by VL, and it differs in that the perpendicular selection line 9 for reset was excluded to the configuration of the example 1 shown in drawing 10 . By vertical-scanning circuit 12A He is trying to impress the electrical potential difference more than a threshold to the gate of MOS transistor 4 for reset like an example 1 through the horizontal scanning line 5 at the time of the charge storage of an optoelectric transducer 1.
[0028] That is, drawing 5 is the circuitry Fig. showing the output

section of the level power-source line 5 in the above-mentioned vertical-scanning circuit 12A. In drawing 5 , the shift register with which 12Aa sends out a shift pulse, and 12Ab The serial object of the inverter and the n channel MOS transistor Qn2 which become with the 1st mentioned later, the p channel MOS transistor Qp1 prepared between the 2nd power-source line, and the n channel MOS transistor Qn1, It is the driver circuit which has the p channel MOS transistor Qp2 prepared between the output terminals 5 of the 2nd power-source line mentioned later and the above-mentioned inverter, i.e., a level power-source line. Moreover, the 1st power-source line for 12Ac to supply the high-level potential VL (H) to the level power-source line 5, The 2nd power-source line for 12Ad(s) to supply the potential VL of a low level (L) to the above-mentioned level power-source line 5 and 12Ae show the 3rd power-source line for supplying the potential VL of middle level (M) to the above-mentioned level power-source line 5. Here The potential VL of the middle level of power-source line 12Ae of the above 3rd (M) is set as the supply voltage in signal read-out more than the threshold of MOS transistor 4 for reset.

[0029] Moreover, drawing 6 is a timing chart for explaining actuation of an example 2, and drawing 7 shows the cross section and potential flow chart of MOS transistor 4 for reset for explaining actuation of an example 2, and explains hereafter actuation of the image sensors which start an example 2 with reference to drawing 6 and drawing 7 . In addition, in drawing 6 , period 1H are 1 level period in the usual television method, and a horizontal blanking interval and period Read-out are equivalent to a signal read-out period for period H-BLK. Moreover, the clock V1 and the clock H1 express typically the clock supplied to the vertical-scanning circuit 12 and the horizontal scanning circuit 11, respectively. Moreover, in drawing 7 , (A) is the cross section of MOS transistor 4 for reset, gate 4a and drain 4b of MOS transistor 4 for reset are connected to the level power-source line 5, and the source field has become an optoelectric transducer 1. Moreover, 4c shows the substrate.

[0030] Now, in drawing 6 , it operates like the conventional example. That is, in time of day T2, if the potential of the level power-source line 5 becomes high-level, potential potential phiPD of an optoelectric transducer 1 will be reset by phiPD=VL(H)-Vthr (H) (refer to drawing 7 (D)). And it goes into are recording mode like [T3 / time-of-day] an example 1 (refer to drawing 7 (C)). At this time, the potential potential of gate 4a of MOS transistor 4 for reset is set as the potential of the low level of the level power-source line 5 shown by VL

so that it may be set to VL(L) >Vthr (O). It was referred to as VL(L) =VL (M) in this example 2. The middle level VL (M) is time of day TO and the supply voltage in signal read-out of T 1:00.

[0031] As shown in drawing 1 , namely, the potential of the level power-source line 6 By driver circuit 12Ab, to the timing reversed to the n+1st shift pulses of shift register 12Aa It becomes the 1st high-level potential VL of power-source line 12Ac (H), and the potential VL of the 3rd middle level of power-source line 12Ae (M). At the time of are recording mode The supply voltage in signal read-out more than the potential VL of the middle level set up by 3rd power-source line 12Ae (M), i.e., the threshold electrical potential difference of MOS transistor 4 for reset, is impressed to the gate of MOS transistor 4 for reset.

[0032] Therefore, MOS transistor 4 for reset cuts off at the time of phiPD>VL(L)-Vthr (phiPD), and the usual are recording actuation is performed. when it comes to phiPD<VL(L)-Vthr (phiPD), MOS transistor 4 for reset should turn on, and lengthen a superfluous charge to drain 4b, and blunder to it -- MOS transistor 4 for reset works as an overflow drain (refer to time-of-day T four shown in drawing 7 (C) and drawing 6).

[0033] Here, the amount Qmax of the maximum stored charge of an optoelectric transducer 1 is {(VL(H)-Vthr (H))- (decided by VL(M)-Vthr(M)}/CPD.).

Vthr which fills Vthr(H);phiPD=VR(H)-Vthr (phiPD) (phiPD)

[0034] According to the above-mentioned example 2, to therefore, the gate of MOS transistor 4 for reset which carried out the series connection to the optoelectric transducer 1 at the time of are recording mode Since it was made to impress the electrical potential difference more than the threshold electrical potential difference of MOS transistor 4 for reset set up by 3rd power-source line 12Ae Like an example 1, as during an are recording period changes MOS transistor 4 for reset into ON condition and the superfluous charge generated in the optoelectric transducer 1 is drawn out to the source side of MOS transistor 4 for reset, a blooming is controlled, and a good image is obtained in a wide range illuminance.

[0035] example 3. -- in this example 3, it plans making unnecessary the power-source line linked to that gate by using as a depression transistor MOS transistor 4 for reset of the example 1 and example 2 which are shown in drawing 10 and drawing 4 . Usually, the SURESHI hold electrical potential difference Vth of an MOS transistor (O) expects the noise margin etc., and, in the case of the NMOS transistor, is set as

Vth(0) >0. Therefore, as drawing 10 and drawing 2 showed, although another power source is required, the low level VR (L) and VL of the perpendicular selection line 9 for reset and the level power-source line 5 (L) the low level of the perpendicular selection line 6 etc., respectively Vthr If (0) <0 [4], i.e., the MOS transistor for reset, is used as a depression transistor, the low level VR (L) and VL of the perpendicular selection line 9 for reset and the level power-source line 5 (L) can be made into a grand level, and the power-source line can be made unnecessary.

[0036] It sets in example 4. and the above-mentioned examples 1 and 2, and is the SURESHI hold electrical potential difference Vthr of MOS transistor 4 for reset. (0) Since it may be smaller than Vth (0) of other MOS transistors, as MOS transistor 4 for reset The thing of the minimum effective gate length L, such as a short channel effect, can be considered as use, and in this example 4, as MOS transistor 4 for reset in the above-mentioned examples 1 and 2, when gate length uses the thing of minimum line width, contraction of a pixel dimension can be enabled.

[0037] He is trying to plan the reduction effectiveness of reset variation in example 5. and this example 5 by making channel concentration of MOS transistor 4 for reset in the above-mentioned examples 1 and 2 equal to the concentration of a substrate or a well. That is, in order that Vth (0) of the usual MOS transistor may give a margin, although acceptor concentration under the gate is made deeper than substrate (well) concentration, by an ion implantation etc., the margin of Vthr (0) is unnecessary, it is being able to decide Vthr (0) of MOS transistor 4 for reset by substrate (well) concentration, and deciding by substrate (well) concentration, and there is effectiveness of being able to reduce reset variation.

[0038] The same effectiveness is done so although PMOS is sufficient as it although the MOS transistor showed the case which is example 6. where it constituted from an NMOS, and a polarity becomes opposite in that case in the above-mentioned examples 1-5.

[0039] Example 7., next drawing 8 show another embodiment of this invention. In drawing 8 , it has the configuration which has stationed perpendicularly the 1st group who added MOS transistor 14 for pixel mixing to the circuit elements 1-6 which constitute the pixel of the example 2 which 14 and 15 showed the MOS transistor for pixel mixing, and 16 showed the perpendicular selection line for pixel mixing (VT), and was shown in drawing 4 , and the 2nd group who consists of an optoelectric transducer 1, MOS transistor 15 for pixel mixing, and a perpendicular selection line 16 for pixel mixing by turns.

[0040] In this circuitry, the transistor 14 (after a field switch is the transistor 15 for pixel mixing) for pixel mixing is turned on after are recording, after mixing the signal charge accumulated in the optoelectric transducer 1 of the 1st and the 2nd group, a signal is read like an example 2 and a reset action is performed. It sets in this embodiment as well as an example 2, and is VL(L) >Vthr at the time of are recording. The same effectiveness as examples 1 and 2 is done so by setting up the low level of the level power-source line 5 so that it may be set to (0).

[0041]

[Effect of the Invention] As mentioned above, the 1st MOS transistor for reset which made the source field the optoelectric-transducer section according to claim 1 of this invention, The 2nd MOS transistor for magnification read-out by which the gate was connected to the above-mentioned optoelectric-transducer section, In the solid state image sensor equipped with two or more pixels which have the 3rd MOS transistor for pixel selection connected to the 2nd MOS transistor of the above at the serial Since the gate of the 1st MOS transistor for reset was equipped with a scan means to impress the electrical potential difference more than the threshold of this MOS transistor, at the time of the charge storage of the above-mentioned optoelectric-transducer section During an are recording period changes the 1st MOS transistor for resetting the above-mentioned optoelectric-transducer section into ON condition. As the superfluous charge generated in the optoelectric-transducer section is drawn out from the source side of the 1st MOS transistor for reset, a blooming can be controlled, and it is effective in the ability to obtain a good image in a wide range illuminance.

[0042] Moreover, according to claim 2, it is effective in the ability to make into a grand level the electrical potential difference impressed to the gate, and make the power-source line unnecessary by constituting the 1st MOS transistor of the above from a depression transistor.

[0043] Moreover, according to claim 3, by making channel concentration of the 1st MOS transistor of the above equal to the concentration of a substrate or a well, a threshold electrical potential difference can be decided by the concentration, and it is effective in the ability to reduce reset dispersion.

[0044] Furthermore, according to claim 4, there is effectiveness of the ability to make a pixel dimension reduce by constituting the gate length of the 1st MOS transistor of the above from minimum line width.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is for explaining the solid state image sensor concerning the example 1 of this invention, and is the circuitry Fig. of the output section of the perpendicular selection line 9 for reset in the vertical-scanning circuit 12.

[Drawing 2] It is a timing chart explaining actuation of the solid state image sensor concerning the example 1 of this invention.

[Drawing 3] It is the cross section and potential flow Fig. of a solid state image sensor concerning the example 1 of this invention.

[Drawing 4] It is for explaining the solid state image sensor concerning the example 2 of this invention, and is a 1-pixel circuitry Fig.

[Drawing 5] It is for explaining the solid state image sensor concerning the example 2 of this invention, and is the circuitry Fig. showing the output section of the level power-source line 5 in vertical-scanning circuit 12A shown in drawing 4 .

[Drawing 6] It is a timing chart explaining actuation of the solid state image sensor concerning the example 2 of this invention.

[Drawing 7] It is the cross section and potential flow Fig. of a solid state image sensor concerning the example 1 of this invention.

[Drawing 8] It is the block diagram of the example of application which has stationed perpendicularly the 1st group who added the MOS transistor for pixel mixing to the circuit which starts the example 7 of this invention and constitutes the pixel of an example 2, and the 2nd group who consists of an optoelectric transducer, an MOS transistor for pixel mixing, and a perpendicular selection line for pixel mixing by turns.

[Drawing 9] It is the circuit diagram showing the magnification read-out mold solid state image sensor concerning this invention and the conventional example.

[Drawing 10] It is the 1-pixel circuitry Fig. of the solid state image sensor concerning the example 1 and the conventional example of this invention.

[Drawing 11] It is a timing chart explaining actuation of the solid state image sensor concerning the conventional example.

[Description of Notations]

1 Optoelectric Transducer, 2 MOS Transistor for Magnification Read-out, 3 MOS Transistor for Pixel Selection, 4 The MOS transistor for reset, 5 A level power-source line, 6 Perpendicular selection line, 7 A perpendicular signal line, 9 The perpendicular selection line for reset,

12 Vertical-scanning circuit, 12a A shift register, 12b A driver circuit, 12c The 1st power-source line, 12d The 2nd power-source line, 12A A vertical-scanning circuit, 12Aa A shift register, 12Ab A driver circuit, 12Ac The 1st power-source line, 12Ad The 2nd power-source line, 12Ae 3rd power-source line